REMARKS

After entry of this amendment, claims 1 and 3 – 20 will be pending. Claims 1, 5, 7, 9, and 13 have been amended to clarify the scope of these claims, and new claims 17 – 20 have been added. Support for the amendments and new claims may be found in the originally filed application in, e.g., the originally filed claims and Figure 4a – 4b and related text. No new matter has been added.

Replacement drawings are enclosed.

Telephonic conference

The undersigned attorney thanks Examiner Huber for the telephonic conference that took place on November 24, 2008. The Examiner's suggestions are reflected in this Response.

Rejection of claims under 35 U.S.C. § 102

Claims 1, 3, 4, 6, 13, and 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,455,905 to Perugupalli et al. ("Perugupalli"). Perugupalli appears to disclose a push-pull transistor having first and second LDMOS transistors formed thereon and configured for push-pull operation, the first and second transistors sharing a common element current region. In a power transistor package, the push-pull transistor chip is attached to a mounting flange serving as a common element ground reference. *See* Perugupalli, abstract.

The Examiner relies on Perugupalli to teach all of the elements of independent claims 1 and 13. Perugupalli, however, does not teach or suggest a structure including two pairs of devices, with a multi-layer metal interconnect structure disposed above each pair of devices, as required by amended independent claims 1 and 13.

Further, Perugupalli does not teach and suggest a first pair of devices and a second pair of devices, each pair of devices having a first source and a second source, such that both first source terminals are connected to both second source terminals to define a common source terminal, with the common source terminal being disposed in a multi-layer interconnect structure disposed above each pair of devices, as recited in amended independent claim 1. Perugupalli also does not teach or suggest connecting, in each pair of devices, first and second drain terminals and first and second gate terminals via the multi-layer metal interconnect structure, as also required by claim 1.

Further, Perugupalli does not teach a multi-layer metal interconnect system including a first electrically isolated lead comprising both first source terminals connected to both second source terminals, as recited in amended independent claim 13.

Rather, Perugupalli appears to describe discrete transistors that include source regions coupled to the surface of the flange, either by a wire bond or a highly doped path through the die. *See*, e.g., Figures 8 and 11 and related text. A common source region 155 is mentioned with respect to Figure 6, but this common source region appears to be a single source shared by two transistors, rather than two source terminals connected to each other, as required by claims 1 and 13. Perugupalli does not teach or suggest (i) multi-layer interconnect structures, and (ii) disposing leads (comprising connections between source terminals of different devices) in multi-layer interconnect structures, as recited in the instant claims.

Furthermore, one of skill in the art would not employ a multi-layer interconnect structure in the devices disclosed by Perugupalli, as that would reduce the functionality of Perugupalli's devices. Perugupalli states that:

> [a]n important factor for stable operation of … high power, high frequency devices [such as the devices disclosed by Perugupalli] is providing a uniform ground reference potential for both power transistors and the surrounding circuitry. In particular, high power high frequency power transistor devices control relatively large amounts of current. Because of the ground path losses for these currents, there is a voltage drop created which causes signal loss, decreased efficiency, and reduced isolation between ports, which in turn reduces stability.

See column 1, lines 24 – 33. Thus, to reduce unwanted voltage drops due to ground path loss, Perugupalli uses multiple source bond wires to connect to the flange (ground reference), with an individual bond wire connecting each source terminal to the flange. On the other hand, as one of skill in the art would recognize, on-chip multi-layer interconnect systems generally have higher resistances that tend to increase the ground path losses. Also, on-chip multi-layer interconnect systems tend to have higher parasitic inductances and capacitances that may contribute to further signal losses. Individual bond wires to the terminals of the multiple transistors, as disclosed by Perugupalli, reduce parasistic inductances and capacitances. Thus, incorporation of a multi-layer interconnect structure, as required by the instant claims, would negatively impact Perugupalli's devices.

Applicants submit that, for at least these reasons, amended independent claims 1 and 13 and claims dependent therefrom are patentable over the cited art.

Rejection of claims under 35 U.S.C. § 103

Claims 5, 7, and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Perugupalli in view of U.S. Patent Publication No. US 2002/0008549 to Forbes ("Forbes"). Forbes appears to disclose a pseudo differential current sense amplifier circuit that facilitates the introduction of hysteresis, enabling differentiation of true signals from noise transients, and conserving circuit design space by allowing for single sided/ended sensing. *See* abstract. The Examiner recognizes that Perugupalli does not teach or suggest first and second gate terminals of a first pair of devices connected to the first and second drain terminals of a second pair of devices, and first and second gate terminals of the second pair of devices connected to the first and second drain terminals of the first pair of devices, as required by independent claim 7 and dependent claim 5. The Examiner relies on Forbes to provide this feature.

Neither of the cited references, however, either alone or in combination, teaches or suggests a multi-layer metal interconnect structure disposed above two pairs of devices, as recited in amended independent claim 7. Rather, as discussed above, Perugupalli appears to describe discrete transistors that include source regions coupled to the surface of the flange, either by a wire bond or a highly doped path through the die. *See*, e.g., Figures 8 and 11 and related text. Forbes is utterly silent about the structural features used to couple the devices he discloses.

Thus, neither Perugupalli nor Forbes teaches or suggests multi-layer interconnect structures, or disposing leads (comprising connections between source terminals of different devices, as well as the drain terminals of the first pair of devices and the second drain terminals of the second pair of devices) in multi-layer interconnect structures, as recited in independent claim 7.

Moreover, one of skill in the art would not combine the connections disclosed by Forbes with the structures disclosed by Perugupalli because such an alteration would render the structures of Perugupalli inoperable. Perugupalli teaches that, to take advantage of the desirable attributes associated with the push-pull amplifier, the characteristics of the two transistors should be very similar. See column 1, lines 37 –39. For example, in an embodiment, the transistor chip 120 of Perugupalli includes two LDMOS transistors having similar characteristics formed on a single semiconductor die 122. *See* column 3, lines 59 – 61. To extend the power handling capability of a

push-pull transistor device, Perugupalli suggests having multiple conduction channels operating in parallel, with activation of the first gate lead facilitating conduction from the first drain lead 143 to the flange. *See* column 4, lines 55 – 60. A preferred push-pull transistor chip 220 disclosed by Perugupalli includes first and second LDMOS transistors, each having multiple channels operating in parallel, fabricated on a single semiconductor die 222. *See* column 4, lines 62 – 66. In these various examples, the paired transistors should operate in parallel.

In contrast, Forbes discloses transistor pairs including a first transistor of a first conductivity type and second transistor of a second conductivity type, with the first and second transistors being coupled at a drain region. *See* Figure 4 and related text. Because the two transistors of Forbes are of opposite conductivity types, they do not operate in parallel, as required by Perugupalli. Perugupalli's devices include similar transistors with paired transistors operating in parallel. Therefore, applying the circuit configuration of Forbes to the devices of Perugupalli would be contrary to the teachings of Perugupalli.

With reference to new dependent claim 18, Applicants note that that even if one were to combine the connections of Forbes with the structure of Perugupalli, one still would not attain a structure with first and second lateral devices having source and drain dopants of the same type, with first and second gate terminals of a first pair of devices connected to the first and second drain terminals of a second pair of devices, and first and second gate terminals of the second pair of devices connected to the first and second drain terminals of the first pair of devices. Instead, the source and drain dopants of the first and second devices of Forbes are of different types.

Applicants submit that, for at least these reasons, amended independent claim 7 and claims dependent therefrom are patentable over the cited art. Further, Applicants submit that dependent claim 5 is patentable for at least the reasons claim 1, upon which it depends, is patentable.

Claims 9 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Perugupalli in view of U.S. Patent No. 4,656,493 to Adler et al. ("Adler"). Adler appears to disclose power MOSFETs that are bidirectional and symmetrical for use in AC circuits, and have low on-resistance, fast switching speed, and high voltage capability. *See* abstract. Conductive gate electrodes 84 and 86 are electrically connected to a common device gate terminal 88. *See* column 8, lines 64 – 65. The Examiner recognizes that Perugupalli does not disclose a fourth electrically isolated lead including first and second gate terminals of a first pair of power transistor devices

connected to the first and second gate terminals of a second pair of power transistor devices, as required by independent claim 9, and relies on Adler to supply this feature.

Neither Perugupalli nor Adler, alone or in combination, teaches or suggests a multi-layer metal interconnect structure, and certainly does not teach or suggest a multi-layer metal interconnect structure including the four electrically isolated leads recited in independent claim 9. Rather, Perugupalli describes device components coupled to each other via a surface of a flange. Adler appears to connect metalized electrodes with device main terminals using a single level of metallization. *See* Figure 3 and related text.

Moreover, combining the connections of Adler with the devices of Perugupalli would render the latter inoperable for its intended purpose. Perugupalli explains that

> [u]sing a push pull topology produces an amplifier with higher efficiency than a single ended design operating at comparable power and frequency levels. The two transistors in a push-pull amplifier design are operated 180 degrees out of phase.

See column 1, lines 19 – 23. The structures of Perugupalli include a push-pull amplifier. *See* column 3, lines 50 – 52. Since, as noted above, the two transistors (or pairs of transistors) operate 180 degrees out of phase, one of skill in the art will recognize that the gates of the two transistors (or transistor pairs) need to be controlled independently, with the signal on one gate operating 180 degrees out of phase with the signal on the other gate. The gates of Perugupalli, therefore, cannot be coupled together, as suggested by Adler and as required by the instant claims.

Applicants submit that, for at least these reasons, amended independent claim 9 and claims dependent therefrom are patentable over the cited art.

Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) as unpatentable over Perugupalli in view of Adler and further in view of U.S. Patent No. 4,472,871 to Green ("Green"). Applicants submit that these dependent claims are patentable for at least the reasons that independent claim 9, on which they depend, is patentable.

Claims 15 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Perugupalli in view of Green. Applicants submit that these dependent claims are patentable for at least the reasons that independent claim 13, on which they depend, is patentable.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all claims are now in condition for allowance.

The Commissioner is hereby authorized to charge Deposit Account No. 07-1700 the fee for Request for Continued Examination of $810. Applicants believe that no other fees are necessitated by the present paper. However, in the event that any fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicants' attorney would expedite allowance of this application, the Examiner is cordially invited to call the undersigned attorney at (617) 570-1806.

Respectfully submitted,

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Reg. No. 44,381

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